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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,755	04/21/2006	Andreas Grundl		3852

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EXAMINER	
MEHARI, YEMANE	
ART UNIT	**PAPER NUMBER**
2838	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/559,755	GRUNDL ET AL.	
	Examiner	Art Unit	
	YEMANE MEHARI	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/07/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Summary

1. This is the first office action on the merits of Application No. 10/599,755 filed on 12/07/2005.

2. The applicant oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

3. Claims 1-12 are pending and have been examined.

4. The invention relates to an electronic assembly for switching electric power. Such electronic assemblies may, for example, be designed as half-bridge circuit to be employed for the realization of inverters or frequency converters in the most different fields of application. This includes the operation of synchronous machines, asynchronous machines, reluctance machines, permanent field machines, or the like, as well as motors and generators

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey et al. (US Patent No. 6,160,696 B1) in view of Wu (US Patent No. 7,528,587 B2).

7. **In regard to claim 1,** an electronic assembly (310, fig. 3) for switching electric power, comprising two power supply buses (the positive and negative power supply buses, fig. 3) spaced from each other between which semiconductor switches (AC1, AC2 & AC3, fig. 3) to be driven by means of a control input (see the semiconductor gate control means on col. 1, lines 24-34 and col. 4, line 61 to col. 5 line 4) are arranged at a power output, for providing electric power, a capacitor arrangement (314, fig. 3) bridging the two power supply buses, which extends at least partially over the length of the power supply buses, two contact layers (452/454 on the positive bus 421 and 458/461 on the negative bus 423, fig. 12) see col. col. 5, line 5 to col. 6 line 47) originating from one each of the power supply buses (421/423, fig. 12) and covering the capacitor arrangement (114, fig. 8) at least partially, with the contact layers comprising free end portions which mutually project one another towards the respective other one of the power supply buses, with the two contact layers (421 & 423, fig. 13, col. 5, lines 42- 52) having a freely accessible contact area each which is adapted for contact making with correspondingly configured power terminals (712 & 714, fig. 13), and with the power output comprising a bus bar which is arranged between the two power supply buses (col. col. 5, line 5 to col. 6 line 47); with the two contact layers having a common covering zone in which they are separated from one another by an insulation (see col. 5. line 42-52); with the two power supply buses (see the parallel power buses 421 & 423, fig. 12) being arranged essentially parallel to one another; with the semiconductor switches which are arranged between the two power supply buses being arranged on a substrate (in this case copper is used as the substrate, see col. 5, lines 53-62) which is [preferably] adapted for contact making with a cooling device (36, fig. 1, for the cooling device details see col. 3, line 66 to col. 4, line 11); with the semiconductor switches being

formed by high-speed switching low-loss field effect transistors (FETs) or by high-speed switching low-loss bipolar transistors with insulated gate terminals (IGBTs) (see col. 1, lines 5-11 and col. 3, lines 55-65) with, in particular, with plane contact sheets which are angled for a height compensation or a lateral compensation being soldered or welded as electrical connection between the printed conductors arranged on the circuit board or the substrate (see col. 5, lines 42-62), or the power supply buses (321 7 323, fig. 6) or the bus-bar (130, fig. 8), respectively, one the one hand, and contact making points of the semiconductors, on the other hand; with the semiconductors having large plane contact making points with a coating of noble metal (in this case copper, see col.5, lines 42-62); with at least two semiconductor switches (AC1, fig. 6) which are connected in series under the formation of a half-bridge (312); each of the semiconductor switches having a control input (G) for the connection with a driving means (140, fig. 9, col. 5, lines 2-4); the first semiconductor switch (AC1- top switch, fig. 3) to be connected with its source terminal (S) to a high voltage potential (321, fig. 6); the second semiconductor switch (AC1- bottom switch, fig. 3) to be connected with its drain terminal (D) to a low voltage potential (VDD); for forming an output (A), the drain terminal (323, fig. 6) of each first semiconductor switch (AC top, fig. 3) being connected with the source terminal (S) of the respective second semiconductor switch (Ac-bottom, fig. 3); and at least one capacitor arrangement (314, fig. 3) being arranged between the high and the low voltage potential respective first semiconductor switches being arranged with their source terminal (S) on a common first metallic conductor rail (321, fig. 6) to be connected with the high voltage potential; respective second semiconductor switches being arranged with their source terminal (S) a common second metallic conductor rail (323, fig. 6) which forms the output, with the second

conductor rail being arranged spaced from and adjacent to the first conductor rail each second semiconductor switch being connected with its drain terminal (D) to a common third metallic conductor rail (132, fig. 12) which is to be connected with the low voltage potential being arranged spaced from and adjacent to the first and second conductor rail ; the capacitor arrangement comprising a back-up capacitor which is connected with the first and the third conductor rail via terminals, which encompasses the first and the second semiconductor switches (AC1…AC3) in such a manner that the semiconductor switches are located spatially between the corresponding conductor rails and the back-up capacitor; the control input (G) comprising a terminal (112, fig. 9) for the connection with the driving means in the area of a first face of the conductor rails and the output comprising a terminal for the connection with an electric load in the area of a second face (452/454) of the second conductor rail , which is located opposite the first face (see col. 4, line 12 to col. 6, line 47); with the three rails (321/323, fig. 6) being mechanically firmly connected with each other by an electrically insulating circuit board (340, fig. 7) and a power output stage (fig. 2) of a driving means for a multiphase electrical machine, characterized in that at least one electronic assembly according to Claim 1 is provided for each phase of the electrical machine (fig. 2), with the electronic assembly being arranged at least along a portion of the circumference of the electrical machine (see col. 3, lines 55-65). Except, Bailey et al. do not disclose a MOSFETs with integrated free-wheeling diodes or with additional external free-wheeling diodes which are connected in parallel with the transistors being employed. However, Shoji et al. disclose a MOSFETs with integrated free-wheeling diodes (22 & 23, fig. 2) or with additional external free-wheeling diodes which are connected in parallel with the transistors (20 & 21, fig. 2) being employed (see col. 3, lines 49-61). One of ordinary

skill in the art would have been motivated to integrate the free-wheeling diodes from Shoji et al.'s invention with Bailey's circuit in order to stabilize and control the inverter. Therefore, at the time of the invention it would have been obvious to those who had ordinary skill in the art to have modified the circuit of Bailey's with that Shoji et al.'s in order to enhance the efficiency and quality of the switching electric power apparatus.

Examiner Notes

Examiner cites particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

The prior art made of record and not relied upon is cited to establish the level of skill in the applicant art and those arts considered reasonably pertinent to applicant disclosure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YEMANE MEHARI whose telephone number is (571)270-7603. The examiner can normally be reached on Monday to Thursday, 8 AM to 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica N. Lewis can be reached on (571)272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Adolf Berhane/
Adolf Berhane
Primary Examiner
Art Unit 2838

/YM/